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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,243	07/17/2003	Ashish D. Alawani	0140111	2882
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FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER LEVI, DAMEON E	
			ART UNIT	PAPER NUMBER
			2841	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/623,243

Applicant(s)

ALAWANI ET AL.

Examiner

Dameon E. Levi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-7 and 9-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 9-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1, 3-7, 9-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al US Patent 5969461 in view of Skipor et al US Patent 5720100 and further in view of Huang et al US Patent 6521997**

**Regarding claim 1**, Anderson et al discloses a module comprising:

a surface mount component situated over a laminate circuit board(elements 10,16, Figs 1-3) the surface mount component comprising a first terminal and a second terminal(elements 20, Figs 1-3) ;

a first and a second pad situated on the laminate circuit board, (elements 18, Figs 1-3) the first pad being connected to the first terminal and the second pad being connected to the second terminal(elements 20,18 Figs 1-3),

a solder mask trench (see trench defined by elements 26, Figs 1-3) situated underneath the surface mount component, wherein a solder mask trench is situated over a top surface of the laminate circuit board(elements 26, 16, Figs 1-3), wherein a bottom surface of the surface mount component and the top surface of the laminate circuit board form a moldable gap (elements 34, Figs 1-3) the moldable gap including the solder mask trench(elements 34,26,32 Figs 1-3), wherein the moldable gap and the

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solder mask trench facilitate a flow of a molding compound underneath the surface mount component.

Anderson et al does not expressly disclose wherein the solder mask trench is filled with the molding compound , or, wherein a solder mask uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench.

Skipor et al discloses an apparatus wherein the solder mask trench is filled with the molding compound(elements 30,13,16 Figs 1-3).

Huang et al discloses an apparatus wherein a solder mask (element 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board(element 10, Figs 1-4), and wherein said solder mask does not cover said solder mask trench(element 16, Figs 1-4).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the molding compound to fill the solder mask trench as taught by Skipor et al in the apparatus as taught by Anderson et al as molding compound tend to improve the connection reliability between the component and the circuit board(see Skipor et al, column 3, line 1- column 4, line 10), and moreover, it would have also been obvious to one skilled in the art to apply solder mask layer on the surface of the circuit board but not the solder mask trench as taught by Huang in order to (1) cover the conductive traces on the surface of the circuit board and(2) to allow the molding compound to flow smoothly between the component and the solder mask trench(see Huang et al column 3, lines 20-65).

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**Regarding claim 3**, Anderson et al discloses the instant claimed invention except wherein the moldable gap is filled with the molding compound.

Skipor et al discloses an apparatus wherein the moldable gap is filled with the molding compound (elements 30,13,16 Figs 1-3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the molding compound to fill the moldable gap as taught by Skipor et al in the apparatus as taught by Anderson et al as molding compound tend to improve the connection reliability between the component and the circuit board, as well as, to facilitate thermal dissipation from the component.

**Regarding claim 4**, Anderson et al discloses further comprising an overmold, the overmold being situated over the surface mount component ( column 2, lines 11-17, Figs 1-3).

**Regarding claim 5**, Anderson et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter ( elements 10, Figs 1-3, see columns 1-8)

**Regarding claim 6**, Anderson et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers ( elements 34, Figs 1-3).

**Regarding claim 7**, Anderson et al discloses wherein the overmolded module is an MCM (elements 10, Figs 1-3, see columns 1-7).

**Regarding claim 9**, Anderson et al discloses a module comprising:

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a surface mount component situated over a laminate circuit board(elements 10,16, Figs 1-3), the surface mount component comprising a first terminal and a second terminal(elements 20, Figs 1-3); a first and a second pad situated on the laminate circuit board(elements 18, Figs 1-3) , the first pad being connected to the first terminal and the second pad being connected to the second terminal, (elements 18,20 Figs 1-3) ;

a moldable gap situated underneath the surface mount component, the moldable gap comprising a solder mask trench (elements 34, Figs 1-3), wherein the solder mask trench is situated over a top surface of the laminate circuit board (elements 26, 16, Figs 1-3), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component(elements 34,26,32 Figs 1-3).

Anderson et al does not expressly disclose wherein the solder mask trench is filled with the molding compound , or, wherein a solder mask uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench.

Skipor et al discloses an apparatus wherein the solder mask trench is filled with the molding compound(elements 30,13,16 Figs 1-3).

Huang et al discloses an apparatus wherein a solder mask (element 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board(element 10, Figs 1-4), and wherein said solder mask does not cover said solder mask trench(element 16, Figs 1-4).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the molding compound to fill the solder mask trench

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as taught by Skipor et al in the apparatus as taught by Anderson et al as molding compound tend to improve the connection reliability between the component and the circuit board(see Skipor et al, column 3, line 1- column 4, line 10), and moreover, it would have also been obvious to one skilled in the art to apply solder mask layer on the surface of the circuit board but not the solder mask trench as taught by Huang in order to (1) cover the conductive traces on the surface of the circuit board and(2) to allow the molding compound to flow smoothly between the component and the solder mask trench(Huang et al column 3, lines 20-65).

**Regarding claim 10**, Anderson et al discloses the instant claimed invention except wherein the moldable gap is filled with the molding compound.

Skipor et al discloses an apparatus wherein the moldable gap is filled with the molding compound (elements 30,13,16 Figs 1-3).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the molding compound to fill the moldable gap as taught by Skipor et al in the apparatus as taught by Anderson et al as molding compound tend to improve the connection reliability between the component and the circuit board, as well as, to facilitate thermal dissipation from the component.

**Regarding claim 11**, Anderson et al discloses further comprising an overmold, the overmold being situated over the surface mount component ( column 2, lines 11-17, Figs 1-3).

**Regarding claim 12**, Anderson et al discloses wherein the overmold comprises the molding compound ( column 2, lines 11-17, Figs 1-3).

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**Regarding claim 13**, Anderson et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers( elements 34, Figs 1-3).

**Regarding claim 14**, Anderson et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter (elements 10, Figs 1-3, see columns 1-8).

**Regarding claim 15**, Anderson et al discloses wherein the overmolded module is an MCM(elements 10, Figs 1-3, see columns 1-8).

**Regarding claim 16**, Anderson et al discloses a module comprising:

a surface mount device situated over a laminate circuit board(elements 10,16, Figs 1-3), the surface mount device comprising a plurality of terminals(elements 20, Figs 1-3);a plurality of pads situated on the laminate circuit board(elements 18, Figs 1-3), each of the plurality of pads being connected to a respective one of the plurality of terminals(elements 20,18, Figs 1-3);

a solder mask trench situated underneath the surface mount device( elements 34, 10, Figs 1-3), wherein the solder mask trench is situated over a top surface of the laminate circuit board(elements 26, 16, Figs 1-3), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component(elements 34,26,32 Figs 1-3).

Anderson et al does not expressly disclose wherein the solder mask trench is filled with the molding compound , or, wherein a solder mask uniformly covers said top surface of



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said laminate circuit board, and wherein said solder mask does not cover said solder mask trench.

Skipor et al discloses an apparatus wherein the solder mask trench is filled with the molding compound( elements 30,13,16 Figs 1-3).

Huang et al discloses an apparatus wherein a solder mask (element 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board(element 10, Figs 1-4), and wherein said solder mask does not cover said solder mask trench(element 16, Figs 1-4).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the molding compound to fill the solder mask trench as taught by Skipor et al in the apparatus as taught by Anderson et al as molding compound tend to improve the connection reliability between the component and the circuit board(see Skipor et al, column 3, line 1- column 4, line 10), and moreover, it would have also been obvious to one skilled in the art to apply solder mask layer on the surface of the circuit board but not the solder mask trench as taught by Huang in order to (1) cover the conductive traces on the surface of the circuit board and(2) to allow the molding compound to flow smoothly between the component and the solder mask trench(Huang et al column 3, lines 20-65).

**Regarding claim 18**, Anderson et al discloses wherein the surface mount device is a leadless surface mount device ( elements 10, Figs 1-3, see columns 1-7).

**Regarding claim 19**, Anderson et al discloses wherein the surface mount device comprises at least one component, the at least one component being selected from the

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group consisting of an active component and a passive component ( elements 10, Figs 1-3, see columns 1-7).

**Regarding claim 20**, Anderson et al discloses wherein the overmolded module is an MCM(element 10, Figs 1-3).

### ***Response to Arguments***

Applicant's arguments with respect to claims 1, 3-7, 9-16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E. Levi whose telephone number is (571) 272-2105. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEL

Dameon E Levi  
Examiner  
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A handwritten signature in black ink, appearing to read 'KAMAND CUNEO', with a large, stylized loop at the end.

**KAMAND CUNEO**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**